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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,019	12/21/2000	Debra Bernstein	10559-268001/ P9023	3295
20985	7590	08/26/2004	EXAMINER RAMPURIA, SATISH	
FISH & RICHARDSON, PC 12390 EL CAMINO REAL SAN DIEGO, CA 92130-2081			ART UNIT 2124	
DATE MAILED: 08/26/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/747,019	BERNSTEIN ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Satish S. Rampuria	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 May 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 and 15-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 and 15-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                                   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>6/4/04</u> .  | 6) <input type="checkbox"/> Other: _____                                    |

***Response to Amendment***

1. This action is in response to the amendment received on 05/17/2004.
2. Claims 1-12, and 15-21 are pending.
3. Claims 13 and 14 are cancelled by the applicant.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-7, 11 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bates et al., hereinafter called Bates, US Patent No. 6,378,125, in view of Wen et al., hereinafter called Wen, US Patent No. 5,956,514.

*As per claims 1, 2, 3 and 4, Bates discloses:*

*- A method of debugging code that executes in a multithreaded processor having a plurality of microengines* (Abstract, "A computer system... method to facilitate debugging of multi-threaded computer program") comprises;

*- receiving of program instruction and an identification representing a selected one of the plurality of microengines* (col. 6, lines 19-23 "the address... exception... found... break point table... then determination is made... address is associated with a thread ID control point") *from a remote user interface connected to the processor* (col. 3, lines 46-45 "obtains instructions, or op code, and data via a network")

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- *pausing program execution*. It is interpreted that program must be paused in order to insert the break point.

- *inserting a breakpoint after a program instruction that matches the program instruction received from the remote user interface* (col. 3, lines 32-34 "Thread identification... break points... user inserted interruptions to program execution" and col. 7, lines 66-67 "the received thread identifier is compared with each thread identification control point see in the received thread has hit one of the thread identification control point")

- *resuming program execution* (col. 5, lines 6-7 "user provides an input that resumes execution of the program")

- *executing a breakpoint routine* (col. 6, lines 44 "break point routine") *if program execution in the selected microengine encounters the breakpoint* (col. 6, lines 11-14 "break point routine... hitting (encountered) break point... determination is made... whether... system... contained... the break point table")

- *resuming program execution in the microengine* (col. 5, lines 6-7 "resumes execution of the program")

Bates did not explicitly disclose plurality of microprocessor and sending interrupt to a selected microengine.

However, Wen discloses a system uses multi processor and interrupt is being sent to the specific processor (Abstract, "Multiple processor application" and col. 6, lines 58-59, "sending an interrupt 0 to a specific processor").

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Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the system uses multi processor and interrupt is being sent to the specific processor as taught by Wen in to the system of breakpoint as taught by Bates. The modification would be obvious because of one of ordinary skill in the art would be motivated to select a processor from multi processor to debug the program.

*As per claim 5*, the rejection of claim 4 is incorporated and further Bates discloses:

- *sending the identification* (col. 5, line 6 "user provide (send) an input") *an interrupt handler* (col. 5, lines 11-12 "An interrupt handler")
- *executing the breakpoint routine* (col. 6, lines 44 "break point routine") *in the microengine* (col. 3, lines 44 "includes at least one processor") *represented by the identification* (col. 4, lines 58-59 "setting a thread identification control point or a break point")

*As per claim 6 and 7*, the rejection of claim 1 is incorporated and further Bates discloses:

- *the data are representative of the state of the threads in the selected microengine* (col. 5, lines 56-58 "This record 47 will include data and to whether the control point is to be a thread identification control point, such as by setting high the thread ID control point flag 54 in FIG. 3")

*As per claim 11*, the rejection of claim 1 is incorporated and further Bates discloses:

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- *breakpoint routine resides in a store of a controlling processor*. It is interpreted that in order to process the breakpoint routine it must be reside in the processor, i.e., control.

*Claim 21* is the product claim corresponding to method claim 1 and rejected under the same reason set forth in connection of the rejection of claim 1 above.

6. Claims 8-10 and 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bates, in view of Wen, and further in view of Mitchell, hereinafter called Mitchell, U.S. Patent No. 6,230,119.

*As per claim 8, 9, and 10* the rejection of claim 4 incorporated and further Bates did not explicitly disclose using a register with certain bits assigned to particular action:

However, Mitchell discloses a processor using a register with having bits assign to perform certain action (col. 5, lines 63-64 "FIG. 8 illustrates the emulation control register, EMUCON, provided within a data processor" and col. 6, lines 29-31 "The sixth bit is an emulation single step, ESS bit which causes the data processor to only execute single instructions between emulator programme operations" and col. 6, lines 9-13 "The fifth bit enables execution... EES register inspected... determine whether the breakpoint instruction should actually be executed"). in an analogous system for break point execution in a debugger.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to processor using a register in to perform certain actions as taught by Mitchell in corresponding to the breakpoint processing

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method for multi processors as taught by the combination system of Bates and Wen.

The modification would be obvious because of one of ordinary skill in the art would be motivated to include the registers in the data processor to execute the tasks during debug operations as suggested by Mitchell (col. 2, lines 9-12).

*As per claim 12*, Bates discloses:

- *perform a breakpoint routine residing in a debug library in one of the contexts* (col. 7, lines 34-37 "The breakpoint manager routine ... would be performing... corresponding action... regard to the breakpoint table (library)"),
- *and resume program execution* (col. 5, lines 6-7 "resumes execution of the program"),
- *the request including a context identification* (col. 7, lines 66-67 "the received thread identifier is compared with each thread identification control point see in the received thread has hit one of the thread identification control point").

Bates does not explicitly disclose a processor can execute multiple context have a register, a counter, and an arithmetic logic unit, a breakpoint in the context points to the breakpoint routine, the breakpoint is inserted into the context in response to a user request received through a remote user interface connected to the processor.

However, Mitchell discloses *a processor that can execute multiple contexts* (col. 3, lines 3-4 "data processor executes emulation instructions (context) using reserved emulation registers") *a register stack* (col. 3, line 7-8 "the stack, which may experience some minor and wholly reversible alterations") *a program counter for each executing context* (col. 5, lines 11-12 "program counter and stack used by user executable code")



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*an arithmetic logic unit* (col. 5, line 57-58 "the processing core (also known as an arithmetic logic unit ALU)") *coupled to the register stack* (col. 5, lines 60-61 "reserved register... include... stack"), *a breakpoint in the context points to the breakpoint routine* (col. 5, lines 10-16 "An interrupt handler... passes information regarding... interrupt to the break point manager 30... updates the break point table 32... as required... to determine what type of control point was encountered and the associated processing"), *the breakpoint is inserted into the context in response to a user request received through a remote user interface connected to the processor* (col. 3, lines 32-34 "Thread identification control points and break points are both examples of control points, which are generally user inserted interruptions to program execution").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made the processor including a register, a counter and an arithmetic logic unit, a breakpoint routine and insert breakpoint into the context in response to user request as taught by Mitchell in corresponding the breakpoint method as taught by Bates. The modification would be obvious because one of ordinary skill in the art would be motivated to have a processor in the breakpoint method and receive a breakpoint from the user to have efficiently debugging the system as suggested by Mitchell (col. 1, lines 49-62).

*As per claim 15*, the rejection of claim 12 is incorporated and further Mitchell discloses:

*- wherein an end of the breakpoint routine points to a program counter of the context* (col. 7, lines 54-57 "During execution of the user programme, the programme counter

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will eventually point to the address 0120 which has the A5 emulation break point instruction written therein in place of the "clear A" instruction")

*As per claim 17*, the rejection of claim 12 is incorporated and further Bates discloses:

- *wherein the breakpoint causes an interrupt* (col. 3, lines 37-38 "Thus, the invalid (breakpoint) instruction causes a hardware interrupt")

*As per claim 18*, the rejection of claim 17 is incorporated and further Bates discloses:

- *wherein an interrupt handler services the interrupt* (col. 5, lines 11-13 "An interrupt handler, or similar means, passes information regarding the exception or interrupt to the break point manager 30")

*As per claim 19*, the rejection of claim 18 is incorporated and further Bates discloses:

- *wherein the interrupt handler identifies the context from the interrupt* (col. 5, lines 15-16 "as required in order to determine what type of control point was encountered and the associated processing")

*As per claim 20*, the rejection of claim 18 is incorporated and further Bates discloses:

- *wherein the interrupt handler identifies a processor identification* (col. 5, lines 15-16 "as required in order to determine what type of control point was encountered and the associated processing")

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*As per claims 3 and 16*, the rejection of claims 1 and 12 are incorporated respectively and further Mitchell disclose:

- *disabling a processor enable bit associated with the selected microengine* (col. 6, lines 9-13 “The fifth bit enables execution... EES register inspected... determine whether the breakpoint instruction should actually be executed”).

Bates did not explicitly discloses breakpoint routine perform at a context switch/swap.

However, Wen discloses the context switch at routine (col. 6, lines 42-45 “The processor register context may be switched between application 64 and the monitor software 46 modes by the appropriate one of two routines from the application context switch CSU 66”).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of context switch as taught by Wen in corresponding to the break point processing method in the combination system as taught by Bates and Mitchell. The modification would be obvious because of one of ordinary skill in the art would be motivated to switch the processor’s attention from one task to another to perform the priority task first.

### ***Response to Arguments***

7. Applicant’s arguments with respect to claims 1, 12 and 21 have been considered but they are not persuasive.

In the remarks, the applicant has argued that:

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For claims 1 and 21 cited reference does not suggest “receiving a program instruction and an identification representing a selected one of the plurality of microengines from a remote user interface connected to the processor, pausing program execution in the threads executing in the selected microengine”, as claimed in 1 and 21.

Claim 12 reference does not suggest “perform a breakpoint routine residing in a debug library in one of the contexts, a breakpoint in the context pointing to the breakpoint routine, the breakpoint inserted into the context in response to a user request received through a remote user interface connected to the processor, the request including a context identification”, as claimed in 12.

Examiner's response:

Regarding claims 1 and 21, it is noted that the rejection clearly points out where Bates and Wen teach the claimed features and why it would b have been obvious to combine their teachings. Applicant only makes general allegations and does not point out any errors in the rejection. Rather, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Therefore, the rejection is proper and maintained herein.

Regarding applicant's arguments with respect to claim 12, the combination of Bates and Mitchell clearly would include the newly added features, as set forth in this office action.

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*Conclusion*

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Satish S. Rampuria  
Patent Examiner  
Art Unit 2124  
08/23/2004



JOHN CHAVIS  
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